

安富利 X-fest 北京站的注册页面

欢迎您来到安富利 X-fest 北京站的中文版注册页面。为了完成注册，您需要填写原本的英文报名表，此文件是在英文版本的基础上增加了中文说明，并提供指引以方便完成注册。您可以使用中文字符填写注册信息。

请注意，所有标有*的栏目为必填项。

完成注册后，您将会收到注册确认电子邮件，请小心检查确保您的所有信息是正确。如果您对注册流程有疑问或需要更新任何信息，请发送电子邮件至 XilinxAPAC@avnet.com。我们的代表会尽快与您联系。

我们热忱期待与您在安富利 X-fest 相见！



Registration: 北京 / Beijing, China
January 12, 2010
Beijing Jingyi Hotel
No. 9 Dazhongsi East Road, Haidian District
Beijing 100098

Attendee Information (出席者资料)

Greeting: * (称呼: *)	<input type="text" value="Please select..."/>
First Name: * (名字: *)	<input type="text"/>
Last Name: * (姓氏: *)	<input type="text"/>
Badge First Name: * (名字(登记证上): *)	<input type="text"/>

Your name will be printed exactly as you type

it here.

Badge Last Name: * (姓氏(登记证上): *)
Your name will be printed exactly as you type it here.

Company Name: * (公司名称: *)
Your company name will be printed exactly as you type it here.

Job Title: * (职位: *)
Your job title will be printed exactly as you type it here.

What is your primary job function? * (您工作的主要职责是: *)

What market segment best fits your company's product offering? * (您公司提供的产品范围是: *)

How did you hear about X-fest? * (您如何知道 X-fest 的讯息? *)

Have you attended an X-fest event in the past? * (过去曾经参加 X-fest? *)

Yes No

Contact Information (联系方法)

Address 1: * (地址 1: *)

Address 2: (地址 2:)

Address 3: (地址 3:)

City: * (城市: *)

State/Province/County: (省/市:)

Postal Code: * (省/市:)

Country: * (国家: *)

Telephone: * (电话: *)

Email Address: * (电子邮箱: *)

Company Web Page: (公司网站:)

http://

Areas of Interest (兴趣范围)

What programmable logic vendor(s) do you currently use? *Check all that apply (您当前选哪些可编程逻辑供应商? *可多选)

- Xilinx
- Altera
- Actel
- Other
- None - New user

Please select the various features or functions that you will likely use in your next FPGA design. *Check all that apply (请选择您下个FPGA 设计将可能使用的各样特点或功能。 *可多选)

- Virtex-6 Family
- Spartan-6 Family
- Other FPGA Family
- PCIe Interface
- High Speed Serial Interface (non-PCIe)
- MicroBlaze or Other Soft Processor Core
 - Video Processing
 - ADC or DAC interface
- External DRAM (DDR, DDR2, DDR3, etc.)
 - External Processor Interface
 - Ethernet Interface

Current Project (当前项目)

Are you currently working on a design? * (您当前有项目在设计? *)

- Yes – New Design
- Yes – Redesign
- No

Estimated production start: * (估计的生产开始时间: *)




Please select...

Estimated Annual Usage (EAU): * (估计每年的产量: *)




Please select...

Courses (课程)




9:00 – 10:15

-  Fundamentals of FPGA-based Video Design
-  Powering Xilinx Virtex®-6 and Spartan®-6
-  Xilinx Networking: 10/100/1000 to Real-Time




10:45 – 12:00

-  Implementing an FPGA-based Peripheral in an Intel® Atom™-based System
-  Interfacing DDR3 and LPDRAM with the Xilinx Spartan®-6 Hard Memory Controller
-  Xilinx FPGA Co-processing with DSP Processors

1:30 – 2:45

-  Designing Products for the Human Experience
-  Designing with Xilinx Spartan®-6 Gigabit Transceivers and the PCIe Endpoint Block
-  High-speed Clocking: Challenges, Pitfalls and Solutions

3:15 – 4:30

-  Designing with the Xilinx Virtex®-6 PCIe Gen2 Endpoint Block
-  FPGA-based Wireless Communications Systems Design
-  Interfacing to an Analog World

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