

安富利 X-fest 深圳站的注册页面

欢迎您来到安富利 X-fest 深圳站的中文版注册页面。为了完成注册，您需要填写原本的英文报名表，此文件是在英文版本的基础上增加了中文说明，并提供指引以方便完成注册。您可以使用中文字符填写注册信息。

请注意，所有标有*的栏目为必填项。

完成注册后，您将会收到注册确认电子邮件，请小心检查确保您的所有信息是正确的。如果您对注册流程有疑问或需要更新任何信息，请发送电子邮件至 XilinxAPAC@avnet.com。我们的代表会尽快与您联系。

我们热忱期待与您在安富利 X-fest 相见！



Registration: 深圳 / Shenzhen, China
January 21, 2010
Marco Polo Hotel
Fuhua 1st Road, Futian CBD
Shenzhen, 518048
[Hotel Web Site](#)

Attendee Information (请填写资料)

Greeting: * (请选: *)

Please select... ▼

First Name: * (姓名: *)

Last Name: * (姓氏: *)

Badge First Name: * (姓名(稳记证倉): *)

Badge Last Name: * (姓(稳记证倉): *)

Company Name: * (公司名稱: *)

Job Title: * (职位: *)

What is your primary job function? * (您最主要的職責: *)

What market segment best fits your company's product offering? * (您的產品最符合哪一個市場區段: *)

How did you hear about X-fest? * (您如何得知 X-fest 的訊息? *)

Have you attended an X-fest event in the past? * (您是否曾參加 X-fest 活動? *) Yes No

Contact Information (联系方炎*)

Address 1: * (地址 1: *)

Address 2: (地址 2:)

Address 3: (地址 3:)

City: * (城市: *)

State/Province/County: (省/州/縣:)

Postal Code: * (郵政編碼: *)

Country: * (國家: *)

Telephone: * (電話: *)

Email Address: * (電子郵件: *)

Company Web Page: (公司網頁: *)

Areas of Interest (兴趣范围)

What programmable logic vendor(s) do you currently use? *Check all that apply (请勾选哪些可编程逻辑供应商? *请勾选)

- Xilinx
- Altera
- Actel
- Other
- None - New user

Please select the various features or functions that you will likely use in your next FPGA design. *Check all that apply (请选择您下个FPGA 设计将可能使用的各种特点或功能 *请勾选)

- Virtex-6 Family
- Spartan-6 Family
- Other FPGA Family
- PCIe Interface
- High Speed Serial Interface (non-PCIe)
- MicroBlaze or Other Soft Processor Core
- Video Processing
- ADC or DAC interface
- External DRAM (DDR, DDR2, DDR3, etc.)
- External Processor Interface
- Ethernet Interface

Current Project (当前项目*)

Are you currently working on a design? * (您当前是否有项目在设计? *)

- Yes – New Design
- Yes – Redesign
- No

Estimated production start: * (估计的生产开始时间: *)

Estimated Annual Usage (EAU): *
(估计每年的产量: *)

Please select...

Courses (课程)

9:00 – 10:15

- Fundamentals of FPGA-based Video Design
- Powering Xilinx Virtex®-6 and Spartan®-6
- Xilinx Networking: 10/100/1000 to Real-Time

10:45 – 12:00

- Implementing an FPGA-based Peripheral in an Intel® Atom™-based System
- Xilinx FPGA Co-processing with DSP Processors
- Interfacing DDR3 and LPDRAM with the Xilinx Spartan®-6 Hard Memory Controller

1:30 – 2:45

- Designing with Xilinx Spartan®-6 Gigabit Transceivers and the PCIe Endpoint Block
- High-speed Clocking: Challenges, Pitfalls and Solutions
- Designing Products for the Human Experience

3:15 – 4:30

- Designing with the Xilinx Virtex®-6 PCIe Gen2 Endpoint Block
- FPGA-based Wireless Communications Systems Design
- Interfacing to an Analog World

Privacy Policy

Avnet respects your privacy. Please refer to the Avnet's Privacy Statement at <http://em.avnet.com/privacy>.

) 睿底吡廡霖措穩隱私权。请参阅安富利的隐私声明<http://em.avnet.com/privacy>)

Submit

(暖傘*)



Copyright © 1995-2009 [Avnet, Inc.](#) All rights reserved.