

安富利 X-fest 臺北站的註冊頁面

歡迎您來到中文版的安富利 X-fest 臺北站的註冊頁面。為了完成註冊，您需要填寫原始的英文報名表，此文件是提供指引以方便完成註冊。您可以使用中文字符填寫註冊信息。

為了方便您的註冊，我們在英文版本的基礎上增加了中文說明。

請注意，任何標有*的信息都是必須填寫的。

一旦完成註冊，您會自動收到電子郵件，確認您的所有信息。請小心檢查確保您的所有信息是正確的。如果您需要任何改變，請發送電子郵件至 XilinxAPAC@avnet.com



Registration: 臺北 / Taipei, Taiwan
January 26, 2010
Venue TBD

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Attendee Information (出席者資料)

Greeting: * (稱呼: *)	<input type="text" value="Please select..."/>
First Name: * (名字: *)	<input type="text"/>
Last Name: * (姓氏: *)	<input type="text"/>
Badge First Name: * (名字(登記證上): *) <i>Your name will be printed exactly as you type it here.</i>	<input type="text"/>

Badge Last Name: * (姓氏(登記證上): *)
Your name will be printed exactly as you type
it here.

Company Name: * (公司名稱: *)
Your company name will be printed exactly as
you type it here.

Job Title: * (職位: *)
Your job title will be printed exactly as you
type it here.

What is your primary job function? * (您工作
的主要職責是: *)

What market segment best fits your
company's product offering? * (您公司提供的產
品範圍是: *)

How did you hear about X-fest? * (您如何知道
X-fest 的訊息? *)

Have you attended an X-fest event in the
past? * (過去曾經參加 X-fest? *)

Yes No

Contact Information (聯系方法)

Address 1: * (地址 1: *)

Address 2: (地址 2:)

Address 3: (地址 3:)

City: * (城市: *)

State/Province/County: (省/市:)

Postal Code: * (區號:)

Country: * (國家: *)

Telephone: * (電話: *)

Email Address: * (電子郵件: *)

Company Web Page: (公司網站:)

Areas of Interest (興趣範圍)

What programmable logic vendor(s) do you currently use? * Check all that apply (您當前選哪些可編程邏輯供應商? *可多選)

- Xilinx
- Altera
- Actel
- Other
- None - New user

Please select the various features or functions that you will likely use in your next FPGA design. * Check all that apply (請選擇您下個FPGA 設計將可能使用的各樣特點或功能。*可多選)

- Virtex-6 Family
- Spartan-6 Family
- Other FPGA Family
- PCIe Interface
- High Speed Serial Interface (non-PCIe)
- MicroBlaze or Other Soft Processor Core
 - Video Processing
 - ADC or DAC interface
- External DRAM (DDR, DDR2, DDR3, etc.)
 - External Processor Interface
 - Ethernet Interface

Current Project (當前項目)

Are you currently working on a design? * (您當前有項目在設計? *)

- Yes – New Design
- Yes – Redesign
- No

Estimated production start: * (估計的生產開始時間: *)

Estimated Annual Usage (EAU): * (估計每年的產量: *)

Courses (課程)

9:00 – 10:15

- Fundamentals of FPGA-based Video Design
- Interfacing DDR3 and LPDRAM with the Xilinx Spartan®-6 Hard Memory Controller

10:45 – 12:00

- Interfacing to an Analog World
- Powering Xilinx Virtex®-6 and Spartan®-6

1:30 – 2:45

- Designing with Xilinx Spartan®-6 Gigabit Transceivers and the PCIe Endpoint Block
- Xilinx FPGA Co-processing with DSP Processors

3:15 – 4:30

- Designing Products for the Human Experience
- Designing with the Xilinx Virtex®-6 PCIe Gen2 Endpoint Block

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(提交)

